AMENDMENTS TO THE CLAIMS

1-4. (canceled)

5. (currently amended) A method of updating a design of a semiconductor chip at a hardware ~~design~~ description language ~~level~~ (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, comprising:

automatically reading and setting a state value of control signals on a ~~percyle~~ per-cycle basis in a template and updating the HDL design with new data;

changing a first predetermined value of the template to be set with the previous cycle state of the control signals; and

executing a test sweep to determine a "don't care" state of the control signals.

6. (canceled))

7. (original) The method according to claim 5, wherein said first predetermined value comprises a first non-zero value.

8. (currently amended) The method according to claim 5, wherein said "don't care" state indicates a state at which a respective control signal of said control signals maintains a value ~~form~~ from its previous cycle.

9-17. (canceled)

18. (currently amended) A method of creating a state machine control logic for a microprocessor, comprising:

providing a template for every function type within the microprocessor, said template being updated as [[s]] a design specification on a per-cycle basis;

at a first function boundary, reading a current functional template from a hardware ~~design~~ description language ~~level~~;

obtaining a control signal from an opcode group, and determining whether the control signal is active;

if the control signal is not active, obtaining a next control signal from the opcode group, and if the control signal is active, selecting a first non-zero value of the template and changing the first non-zero value to be set to the previous state of the control signal;

searching a data base to locate all tests that have a function of said control signal and creating a test sweep;

updating by a new template, a temporary copy of ~~the~~ an updated microcode function block;

running the test sweep with the previous state set for the ~~one~~ control signal; and

if the test sweep passes, ~~making the~~ marking a control bit as a potential "don't care" value.

19. (currently amended) The method according to claim 18, further comprising:

examining and processing each control signal, setting each one individually, and running a test sweep automatically, to maintain the control signals found to be "don't care" and not setting function-critical signals;

after the template is fully swept on a per-bit basis and when all opcode groups are examined, setting all valid "don't care" bits;

re-running the test sweep to ensure that there is no bit-to-bit interconnections;

incrementing the function count, and creating a new template; finding tests, and completing analysis;

upon the function count reaching a maximum value, every function type being updated with the previous control signal;

executing all templates on the microcodes together with each other;

executing a full regression to ensure that the opcode function ~~sill~~ still functions with the automatically-generated "don't care" verilog, and performing debugging if the regression fails;

if the full regression passes, then designating the new verilog as an official release design, and printing the templates in a readable format so that a complete documentation

exists on a function-by-function basis of true ~~"Os"~~ "O's", true ~~"Is"~~ "1's", and previous "don't care" ~~function~~ functions on a bit-by-bit basis.

20. (canceled)

21. (currently amended) A signal-bearing medium tangibly embodying a program of machine readable instructions executed by an apparatus to perform a method of updating a design of a semiconductor chip at a hardware ~~design~~ description language ~~level~~ (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, said method comprising:

automatically reading and setting a value of control signals on a per-cycle basis in a template and updating the HDL design with new data;

changing a first predetermined value of the template to be set with the previous cycle state of ~~the~~ a control signal; and

executing a test sweep to determine a "don't care" state of the control ~~signls~~ signals.

22. (canceled)